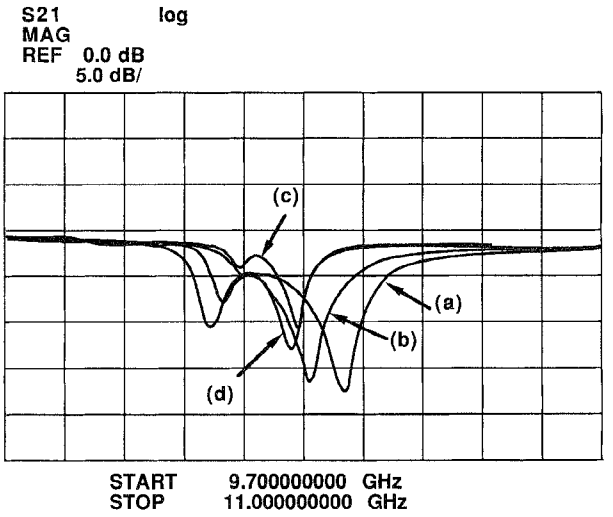

Fig. 4. S21 as a function of frequency for four circuits with identical microstrip and ring resonator dimensions: (R2=2.05 mm, R1=1.58 mm, D=6 35 mm, w=0.470 mm, fo=10 4 GHz, h=0.508 mm) but with different separation distances: (a) d =50.8 μm, (b) d =125 μm (c) d =254 μm, and (d) d =381 μm.

of Fig. 2(a) and (b) are combined to calculate the S_{21} of the overall circuit. For this case, the calculated phase difference came out to be 130° which is very close to the measured value of 126°. Considering the approximations made in determining the circuit elements, the closeness of the measured and calculated phase values also confirms the validity of the even- and odd-mode coupling models presented here.

V. Conclusion

In this paper, the presence of two closely spaced but distinct resonance frequencies of a ring resonator side coupled to a microstrip line are identified as due to the even-mode and odd-mode coupling. The coupling coefficients calculated from the piecewise modeling of the equivalent circuits using the coupled line parameters and the experimentally measured values are in close agreement with each other and verify the presence of the two coupling mechanisms.

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The Use of Active Traveling-Wave Structures in GaAs MMIC's

S. Gareth Ingram and J. Chris Clifton

***Abstract*—A coplanar waveguide has been fabricated on a modulation doped GaAs substrate in order to evaluate the potential of traveling-wave structures in microwave applications. The use of a Schottky contact center conductor enables the line to function as a slow wave structure in which the rf propagation characteristics can be modified with a dc bias. Measurements are reported at 10 GHz on simple structures, some of which incorporated an additional dielectric layer. Results show that slow-wave factors of between 8 and 24 are readily obtained with a loss per slow-wave factor was about 0.7 dB/mm. The practical issues relating to the application of such structures in phase shifters, chip size reduction, compact active filters and resonators are examined.**

I. Introduction

The integration of active traveling-wave structures as planar control components into GaAs monolithic microwave integrated circuits (MMIC's) may provide the means to reduce chip size and increase functionality. At lower frequencies the cost savings could be significant. Traveling-wave structures are transmission line structures which have cross sections analogous to a particular electronic device. The stripline is an example of a nonactive traveling-wave structure, with a cross section based on the parallel plate capacitor. For most purposes, this structure can be considered as a linear transmission line, with propagation properties independent of the rf signal amplitude and any additional dc bias. In contrast, active structures based on junction devices display a marked variation in rf signal propagation with changes in the signal amplitude. For small rf amplitudes, a superimposed dc bias can be used to control the attenuation and electrical length of such a line. Larger signals lead to nonlinear behavior, resulting in pulse shaping, shock wave generation, or even wide-band amplification.

This paper reports on the design and fabrication of Schottky contact transmission lines (SCTL) and metal insulator semiconductor transmission lines (MISTL's) on GaAs to investigate the potential for reducing chip size and for providing voltage-variable signal propagation characteristics.

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II. Schottky Contact Transmission Line

The SCTL structure has been shown to support slow-wave propagation when the substrate incorporates a buried layer with suitable conductivity [1]–[3]. The technique, as used in this work, is based on the fabrication of a coplanar waveguide on GaAs which incorporates a buried n^+ layer. Since the electric component of the signal will not penetrate this low impedance layer it becomes confined to a narrow region between the metalization and buried layer. A solution of Maxwell's equations shows a range of possible propagation modes, depending on the doping level and signal frequency. At low frequencies and low doping levels the signal propagates as a quasi-TEM wave, at high frequencies and doping levels, the signal propagates as a surface wave. Between these regimes, a complex mode of propagation exists in which the electric and magnetic fields are spatially separated, leading to an enhanced effective dielectric constant and a reduced wave velocity. For this reason, these devices are referred to as slow-wave structures, where the slow-wave factor, β is defined as the relative decrease in propagation velocity compared with a microstripline. Several theoretical investigations of these lines can be found in the literature, including the quasistatic approach [4]–[5], spectral domain approach [6], [7], full wave analysis [8], a lumped element model [9], and a brief review of computational methods in [10].

In the design used here, the ground planes of the coplanar waveguide double as ohmic contacts to form a low resistance connection to the underlying n^+ layer. A schematic of the structure is shown in Fig. 1. The use of a lightly doped region immediately underneath the signal conductor, provides a depletion capacitance which can be controlled by applying a dc bias voltage between the conductors. Since the buried n^+ layer acts as a ground plane, the line behaves more like a stripline than a coplanar waveguide, albeit with voltage-variable propagation characteristics. A benefit of this structure is that miniaturization is not limited by the thickness of the substrate. Test structures were grown using MBE on UN GaAs (100) substrates. An UN GaAs buffer layer was grown to establish a high quality growth surface, followed by 2.5 μm of n^+ type GaAs Si doped 7×10^{17} cm^{-3}. This was followed by 2.5 μm of n type GaAs Si doped 4×10^{16} cm^{-3}. Metallization was defined using standard lithography and lift-off techniques to define a set of coplanar waveguides with lengths in the range of 0.5 mm to 2 mm. The ohmic contacts were formed from AuGeNi annealed at 450°C, while the center conductor consisted of 250 nm of Au evaporated over a thin NiCr layer to improve adhesion. The width of the center conductor and the separation from the ground planes was varied in the range 20 μm to 100 μm. The center conductor forms a Schottky contact with the underlying n-type layer and hence forms a depletion region near the surface. To modify this behavior, some devices were fabricated with a dielectric layer between the GaAs surface and the center conductor. This was achieved using a similar lift-off process thermally evaporated from a powder source to produce either 125 nm GeO_x or 250 nm SiO_x $(1 < x < 2)$.

III. Device Testing

Fig. 2 shows a photomicrograph of two 620 μm long SCTL's fabricated with center conductor widths of 40 μm and 20 μm. The coplanar layout of the lines enabled measurements to be made using on-wafer rf probing. The "rough" areas are the annealed ohmic contacts. The conductor thickness was 250 nm, it was not increased by electroplating as conductor losses were not expected to be dominant. For comparison, an identical set of test structures were fabricated on UN GaAs substrates, with a characteristic impedance of 50 Ω. To extend the voltage range, some devices were fabricated with a

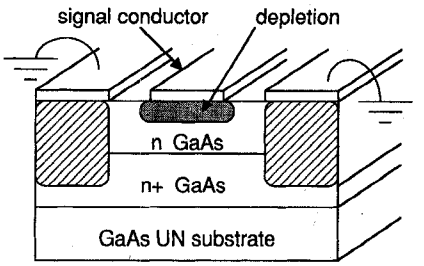


Fig. 1. Schematic of the slow-wave structure consisting of (from the bottom) an UN GaAs substrate, n^+ layer 2.5 μm Si doped 7×10^{17} cm^{-3}, n layer 2.5 μm Si doped 4×10^{16} cm^{-3} and 2.50 nm NiCr/Au metallization.

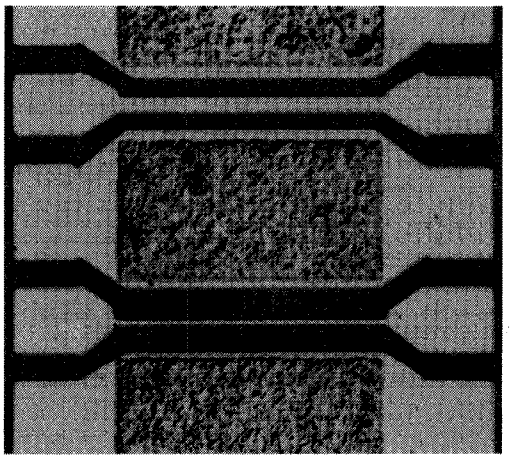


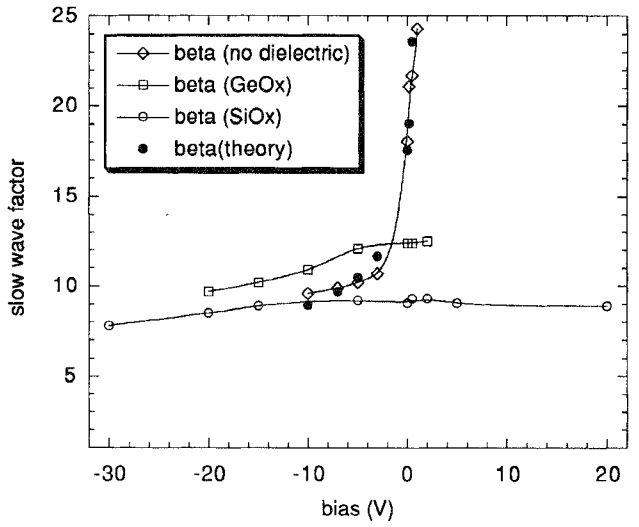
Fig. 2. Photomicrograph of completed device, showing two lines of different widths.

dielectric layer underneath the center conductor, forming a metal-insulator-semiconductor transmission line (MISTL).

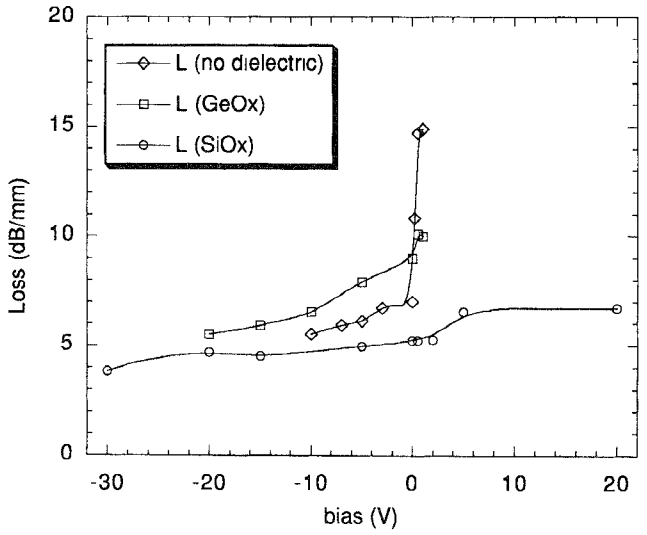
The line impedance, Z_0, is determined by the relative dielectric constant and the ratio of the center conductor width to the distance between it and the n^+ ground plane [11, p. 410]. As this ratio is $\gg 1$, the variation in Z_0 between lines of different widths was negligible. Furthermore, in the slow-wave mode, the effective dielectric constant, ϵ_{eff}, is greatly enhanced, $(\beta \propto 1/\sqrt{\epsilon_{\text{eff}}})$ which leads to a further reduction in the characteristic impedance. This leads to a poor match with the 50 Ω measurement equipment. Hence, de-embedding to obtain the insertion loss, L, directly from the S-parameter measurements was done using $L = 10\,\text{LOG}\,10\{S21^2/(1 - S11^2)\}$. The network analyzer was calibrated over the range 0 to 10 GHz, applying the dc bias through a suitable decoupler. Measurement of line losses are complicated by unquantified radiation losses. By testing identical lines of different lengths (0.62 mm and 1.44 mm) it was possible to subtract out such losses [12].

IV. Results

The measured vairation of phase delay and insertion loss were found to increase with frequency as expected, with losses dominated by those arising from the low impedance semiconductor. Identical transmission lines fabricated on undoped substrates were relatively loss free and showed the expected linear dependence of phase delay with frequency. The quantitative behavior of the phase delay for the active lines depends on the extent of the depletion region, which varies approximately as the square root of the applied dc bias. For the structure used here, a 0–90° phase shifter at 10 GHz is realized with a line length of 380 μm, giving an insertion loss of $L = 3.8$ dB, a maximum sensitivity of 28° V^{-1} and a maximum change in slow-



(a)



(b)

Fig. 3 Bias dependence at 10 GHz of (a) slow wave factor, and (b) insertion loss.

wave factor from $\beta = 8$ to 24 with a characteristic impedance of 3 Ω.

The variation of β and L with dc bias at 10 GHz for both SCTL's and MISTL's is shown in Fig. 3(a) and 3(b), respectively. Since $\beta \propto 1/\sqrt{\epsilon_{\text{eff}}}$ and $\epsilon_{\text{eff}} \propto$ capacitance, by treating the SCTL as a diode (see Appendix) it is possible to write $\beta \propto 1/\sqrt{\sqrt{(0.7\text{ V})}}$. A comparison between this simple model and the measured data is shown in Fig. 3(a), where the calculated values are shown as solid circles. It can be seen that the incorporation of 250 nm of SiOx increases the dc operating voltage range by a factor of three and reduces the maximum L and β by a similar amount. This corresponds to a maximum electric field strength in the oxide of approximately 2×10^6 V cm^{-1}, which in principle could be improved by a factor of five by using a high quality PECVD oxide. The devices incorporating 125 nm of GeOx have a correspondingly smaller breakdown voltage, giving a factor of two improvement over the Schottky contact. It is well-known that GaAs/oxide interfaces have a high trap density, which reduces the influence of the center conductor voltage on the extent of the depletion in the underlying semiconductor. Therefore, a

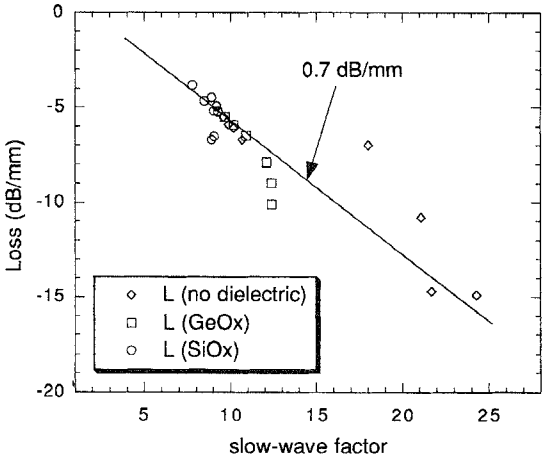


Fig. 4. Variation of insertion loss with slow wave factor at 10 GHz.

detailed understanding of the changes in the rf propagation properties of the lines will also be dependent on the exact nature of the oxide deposition process which will not be considered here.

The relationship between L and β at 10 GHz is shown in Fig. 4. It can be seen that there is a correlation between L and β, although the detailed relationship is nontrivial. This implies that the loss per wavelength is roughly constant, with $L/\beta \approx 0.7$ dB/mm. This compares favorably with 1.8 dB/mm observed by other workers [13].

V. Application to MMIC's

The wafer structure and processing of MMIC's places a number of constraints on the integration of slow-wave structures which may not offer the flexibility to optimize their design. Therefore, it will be necessary to reach a compromise design for use in a particular MMIC. For example, the structure used in this work is similar to the collector structure in a heterojunction bipolar transistor which consists of an n-type collector on top of an n^+ sub-collector. However, the practical issues not only relate to the wafer and processing requirements, but to inherent limitations such as losses and distortion. Since these factors are specific to each application, they are discussed separately.

A. Delay Lines and Pulse Shaping

The use of a SCTL's for voltage-variable delay lines has been investigated by a number of workers [12], [13]. However, the commercial exploitation of such devices is virtually unknown. This is mainly due to the excellent performance already available from traditional p-i-n diode and FET-based phase shifters [14]. Their use in phased array radars for example, favors discrete, digitally selected phase delays rather than continuous adjustment [15]. However, digital designs often occupy a relatively larger chip area, particularly if a large number of bits is needed to achieve the desired resolution. Therefore, for certain applications, the use of slow-wave analog delay lines can be desirable. High rates of phase change per volt obtainable from SCTL's operated close to zero dc bias mean that relatively small control voltages can be employed. However, this can result in distortion of the signal due to the nonlinear nature of the line. Therefore, in practice, it is preferable to shift the operating point to a negative bias in order to reduce the distortion. A common technique used to quantify the distortion is to measure the relative amplitude of the intermodulation products generated when two signals of equal amplitude but slightly different frequencies are applied to the input. If the line behaves like a lumped element diode, the distortion for small signals can be estimated analytically (see Appendix). Thus, a

maximum of $C/I_3 \approx -30$ dBc at a signal level of 15 mW, requires that $V_{dc} < +0.1$ V. The MIS lines exhibit negligible distortion because the high frequency capacitance is relatively insensitive to the applied bias. Therefore the SCTL is the most suitable for phase shifting applications.

The insertion loss was found to be fairly insensitive to bias for the SiOx MISTL. However, the SCTL showed a strong variation of insertion loss with dc bias, particularly near zero bias. This can be compensated for by using a simple single FET-based analogue attenuator. The measured loss @ 10 GHz (zero bias) was 7 dB/mm, which compares favorably with a loss of 26 dB/mm reported by other workers for a similar structure [13].

At large amplitudes, the nonlinear behavior of the slow-wave structures can be exploited for pulse forming. The temporal and spatial modulation of the depletion capacitance of a slow-wave line as the wave travels along the structure results in temporal compression of the input signal. Hence, relatively slow transition times can be made much faster. There will be a trade-off between compression and loss due to excessive line lengths, but a compression ratio of 1:1000 is not unrealistic [16], [17].

B. Space Reduction

Potential savings in chip size are anticipated if the size of transmission line components can be reduced. Using an SCTL or MISTL as a slow-wave structure, it should be possible to reduce line lengths by the slow-wave factor. In this work, values of β in the range 8 to 24 were demonstrated at 10 GHz, which compares favorably with $\beta = 14$ (zero bias) reported by other workers for a similar structure [13]. For X-band power amplifiers a $\lambda/4$ (90°) line would need to be approximately 2 mm long, but with $\beta = 5$ this could be reduced to 400 μm. However, in order to ensure distortion remains better than C/I$_3$ = −30 dBc it will be necessary to operate the SCTL's at low power and a negative dc bias. In power applications the MISTL offers the benefit of low distortion and a low characteristic impedance for matching to active devices. Furthermore, the MISTL structure is directly compatible with many existing commercial processes, making it ideally suited to MMIC manufacture.

Other nonvariable low loss slow-wave structures based on complex multi-level striplines and meander type waveguides proposed by a number of authors [18], [19], require extra processing, which increases the complexity and negates the cost advantages.

C. Compact Filters and Resonators

The slow-wave structure also offers the possibility of low area broadband tunable filters, which are presently realized using gyrator (active) techniques [20], [21] which tend to be inefficient and intolerant to temperature variations. Conventional passive filter types may be fabricated using slow-wave transmission lines, utilising open and shunt circuit stubs. However, the size requirements of normal passive filters makes MMIC realization costly, whereas, a slow-wave structure would not only be compact, but allow the center frequency to be determined electronically [12] with a suitable dc bias applied via an rf block. However, there will be a reduction in Q caused by higher line losses when compared with ordinary stripline resonators. For a simple resonant line this is $Q \propto \omega_0 C Zo/L$ [11, p. 251-259]. Hence, $Q_{slow}/Q_{50\Omega} \approx \beta Z_{slow} L_{50\Omega}/Z_{50\Omega} L_{slow}$ where the subscripts refer to the MISTL and a standard 50 Ω stripline, respectively. With $L_{slow}/\beta \approx 0.7$ dB/mm and $L_{50\Omega} = 0.25$ dB/mm this gives $Q_{slow}/Q_{50\Omega} \approx 1/48$ increasing to 5/2 if Z_{slow} is increased to 50 Ω. Thus the Q-factor does not vary with bias and offers significant size reduction. This would make the SCTL and MISTL suitable for reducing component size where Q is not critical, offering a low power alternative to conventional designs [20], [21].

VI. Conclusion

A simple slow wave structure based on a modulation doped GaAs substrate has been fabricated and measured over the range 0 to 10 GHz. The results indicate that such structures can be used as transmission lines when a reduced signal velocity is desired. In this work, a slow-wave factor of 8 to 24 has been achieved at 10 GHz with a loss per slow-wave factor of 0.7 dB/mm. By employing a dc control bias it was shown that the slow wave factor and insertion loss can be continuously varied over a wide range. The bias dependence of the slow-wave factor was found to be strongly influenced by the addition of a dielectric layer underneath the signal conductor. This provides the means to tailor the characteristics of the lines to suit a specific application. The trade off between the slowing factor, the insertion loss and the dc bias sensitivity has been examined in the context of MMIC circuits. It was found that slow wave structures can, in principle, be designed to give a number of benefits when used as voltage variable delay lines, reduced length transmission lines, and compact variable filters. Improvements in many of these applications are possible if the characteristic impedance of the lines can be increased from 3 Ω to nearer 50 Ω. Further work is required to examine the performance of such structures when the limitations of a particular MMIC process are included in the design.

Appendix

When the stripline is much shorter than the wavelength (as in the case here at 10 GHz), a simple lumped element model may be used. The intermodulation distortion of the SCTL can be estimated by treating it as a reversed biassed abrupt diode where the nonlinear behavior is dominated by the voltage dependent capacitance, $C(V) = C_{jo}/\sqrt{(1 - V/\phi)}$, in which ϕ is the built-in junction potential, C_{jo} the flat-band capacitance and $V = V\,\mathrm{dc} + V\,\mathrm{rf}$ where $V\,\mathrm{rf} = A(\cos\omega_1 t + \cos\omega_2 t)$. The current that flows through the junction is then described by $i = C\ d\mathrm{V}/dt$, which is expanded using a Taylor series

$$i(t) = \sum_{m=1}^{m=\infty} \frac{C_{m-1}}{m} \frac{d}{dt} (V\mathrm{rf})^m \tag{A1}$$

where

$$C_m = \frac{1}{m!} \frac{d^m}{dv} C(V\,\mathrm{dc}).$$

By expanding each order in turn it is possible to identify the amplitude of higher order terms [22, p. 89] for signals at ω_2 and $2\omega_2 - \omega_1$. The ratio of the square of these currents gives

$$C/I_3 \approx 40\,\mathrm{Log}_{10}\{(3/4\sqrt{2})\sqrt{(Z_o P)/(\phi - V_{dc})}\} \tag{A2}$$

where P is the rf input power in W, Zo is the impedance (3 Ω), ϕ the built in potential of the junction (≈ 0.7 V) and V_{dc} the applied dc bias.

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Finite-Difference Time-Domain Analysis of Flip-Chip Interconnects with Staggered Bumps

Hussein H. M. Ghouz and El-Badawy El-Sharawy

***Abstract*— This paper presents finite-difference time-domain (FDTD) analysis of flip-chip interconnects. Transition between coplanar waveguides on the chip and the mother board are investigated over a broad band of frequency by means of Fourier transform of the time-domain results. Objectives of the analysis include the evaluation of bump reflection and insertion loss as well as the reconfiguration of the transition to improve package performance. Novel designs have been developed and presented to reduce the effects of package discontinuities and asymmetry. Staggering the bumps has been found to reduce reflection and insertion loss over a broad band of frequency. A reduction in bump reflection of up to 8 dB per transition can be achieved by staggering the ground and signal connects. The degradation in package performance due to structure asymmetry is also studied. The present designs have been also found to reduce the effects of flip-chip asymmetry on insertion and reflection losses.**

I. Introduction

Coplanar waveguide structures (CPW's) are important planar transmission lines in microwave and millimeter-wave integrated circuits. Analysis of CPW lines has been performed using the finite-difference time-domain (FDTD) method to predict pulse response of the line [1]–[5]. Such a transmission line offers several advantages over the conventional microstrip for monolithic and hybrid microwave integrated circuits (MMIC) applications [5]. These advantages include the ease of parallel and series insertion of both active and passive components and high circuit density. Using CPW in MMIC eliminates the need for the costly back process which includes thinning the substrate, via hole etching and metallization. Typically, 30% of GaAs chips are lost in this process alone.

The popularity of CPW in MMIC applications resulted in increased interest in flip chip packaging due to the compatibility between flip-chip applications and CPW circuits. Flip chip is emerging as the lead technology in multichip module packages [6]–[9]. Several chips can be mounted together to a mother board using flip chip to increase density, improve system performance and reduce cost. This packaging technique also allows combinations of active and passive devices, silicon and gallium arsenide, and probably analog and digital circuits in the same application. In fact, transitions in flip chip coplanar waveguide structure involve the use of metallic bumps to transmit the signal between the chip and the package. The geometry and design of the bumps constitute the basics of flip chip interconnects. These bumps represent a discontinuity to the signal propagating on the line which results in partial loss, reflection and possibly distortion of the signal. In addition, due to misalignment between the mother board and the chip and possible unequal degradation of solder connects, asymmetry of the lumps may result. This can occur, in particular, when large bumps (2 mils or more) are used to align very small bumps (half a mil or less) [10]. As a result, the conventional CPW mode (the odd mode) may couple to undesired modes (the even mode) [11].

This work is mainly concerned with the FDTD analysis and evaluation of frequency dependent parameters of the transition between two coplanar waveguides on two separate substrates connected via metallic bumps. The objectives of the present model is to investigate

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